Research Article

Sustainability of High Temperature Polymeric Materials for Electronic Packaging Applications

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Abstract
Development of polymeric packaging materials for electronic devices have attracted discussions in many published works amid challenges in high speed electronic performance. In order to achieve hybrid integration in most power system, sustainable packaging materials with high thermal conductivity are needed to achieve this purpose. In this paper, attempts were made to analyse the existing packaging materials and the modification of electronics system using 2-D and 3-D dimensional packaging approaches. Also introduced in this work is the integration of polymer multi-functional block in electronic packaging which is aimed at reducing the density of electronic devices. It is hoped that the recommendation from this work will stimulate novel research and generate new interest in applications of sustainable materials for the electronics packaging industry.

Keywords: Insulation materials, Electronic devices, Polymeric packaging, Components density, High temperature

1 Introduction

Heat losses in electronic devices remain unaccounted for as high voltage continues its passage through smaller, faster packages of integrated circuits. Improvement in dielectric materials with high temperature resistant has been ongoing in many published works but the performance of these materials are still limited as shown in Table 1 [1], [2]. Insulation materials have been widely used to protect heat dissipation in huge electrons transfer through conductors involving high speed electronics in an integrated circuits. Findings from other works have shown that sustainable packaging materials have not been rightly utilized in many electronics

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Table 1: Dielectric film candidates for elevated temperature wound capacitors [8]

Dielectric Material	Manufacturing Source	Inherent Properties
Polysilseqioxane	David Sarnoff Labs	Can withstand electrical resistance up to 250°C
Polybenzimidazole	Hoechst	Thermoplastic in nature: good thermal stability above 300°C
Organo-ceramic hybrid nanocomposites	Garth Wilkes, VPI	Resistant to ionizing radiation with high thermal stability
Teflon Perflouroalkoxy	Dupoint	Excellent Mechanical properties with good electrical properties up to 200°C

applications [3]–[5]. Selection of right combination of materials to serve as thermal interface in most elevated temperature above 200°C is often a challenge in most electronic devices [6]. Amin, *et al*. defined high temperature electronics as devices that operate at temperatures above 400°C and hence, the need to establish interconnection and suitable environment for these devices (SiC or Si) to operate above this temperature [7].

In order to test the reliability of most insulation materials, several tests have been advanced to ascertain the integrity and sustainability of these materials in the face of high temperature conditions [9], [10]. One of the frequently used test is Surface Insulation Resistance (SIR) where the electrical resistance inherent in the two servicing conductors are separated using dielectric materials under very high temperature and humidity [11].

The specific reason for SIR test is basically to analyse the integrity property of polymeric packaging materials, and to process the thermal properties of these materials for electronic packaging application [12]. Researchers and other workers in the field of low density polymeric materials are currently working towards newer and lightweight materials for electronic packaging [13], [14]. This has led to more reliable insulating materials to cope with high speed switching in electronics and integrated circuits [15], [16]. The introduction of nanocomposite polymeric materials for electronic packaging has improved the quality of packaging materials coupled with its potentials to dissipate heat under a very tense temperature [17], [18].

The interconnection for these electronic devices sometimes require high temperature operating conditions thereby rendering the existing dielectric materials outdated [19]–[21]. In electronic systems, polymeric materials are commonly used as insulators to reduce heat losses in high thermal conductivities devices and some of these polymeric materials include polyethylene (PE), poly tetra-flouro ethylene (TEFLON), polyester, polyvinyl chloride (PVC), polyethylene-2, 6-Naphthalene Di carboxylate (PEN). Some authors have emphasised the need to incorporate nanoparticles into these polymeric materials in order to strengthened their properties in electronics and integrated circuits system [22]–[24].

Nanocomposites are generally made up of polymer matrices and the introduction of carbon nanotubes in order to enhance its application in electronics packaging [22], [25]–[27]. The role of carbon nanotubes in nanocomposites is basically to raise the thermal properties of the existing composite for packaging application. Part of the experimental works reported by Jones, *et al*. showed that heat dissipation in electronic devices is often noticeable with interface materials experiencing failure as a result of excessive temperature conditions [28]. Some other authors have reported the most negative impact of carbon nanotube in nanocomposite [1], [29]. Key of the pressing challenge is the fabrication of nanocomposite with nanotube as filler. It has been shown in many published works that nanotubes find it difficult to disperse uniformly in polymer matrix [30]–[33]. Although, the blending process have improved but the alignments of carbon nanotubes in the polymer matrix is still a tedious task [34], [35]. Also of great concern is the interaction of carbon nanotube in the polymer matrix and the nature of the connecting interface.

This effect is seen to negatively impact on the formation of the nanocomposite and the overall performance of nanocomposite material for electronic packaging [36]. Organic polymeric materials have also been investigated in other published works for electronic packaging [4], [37]. The use of organic polymeric materials is mainly applicable in the fabrication of Multichip Modules (MCM) for electronic packaging. Although polymeric materials (organic) have been widely explored as a result of their attractive

advantages, i.e., ease of production and low dielectric constant, this materials is also reported to have its shortcomings when compared with the inorganic materials [38]. Key of the attractive property of any polymeric packaging materials is its resilience to withstand high temperature associated with electronic devices [39].

One of the highly favoured polymeric material in microelectronics applications is polyimides. This material is characterised with rigid and semi-rigid aromatic property, demonstrating several combination of thermal and mechanical properties [40]. Key of the findings reported by Hedrick, *et al*. indicates that polyimides exhibits low thermal expansion coefficient coupled with high modulus and tough ductile mechanical property [41]. Several other authors also affirm that their properties are largely retained at 400°C, above which a sudden softening or degradation is observed in some studies [22], [42]. This salient property demonstrate the prospect of this material to retain high degree of molecular order for electronic packing.

2 Existing Packaging Materials and Their Limitations

For a long period time, there has been two types of packaging materials for electronics devices. These are non-hermetic (plastic) and hermetic (metal and ceramic) materials [43]. Non-hermetic packaging materials are the most widely used in view of their low cost and tendency to be sharpen to small size compared to hermetic packaging materials. In terms of cost, non-hermetic materials are also lower than hermetic materials [44], [45]. In a non-hermetic packaging materials, the electronic device is encapsulated in a polymer materials, which is often called encapsulant, as this process is mainly an electrically insulating material that shield the electronics from the negative effects of heat and thermal storage. In the last forty years, lead frame with a 2.5 mm pitch was mainly used, until recently where there is reduction in the size of lead frame to about 1.27 mm pitch which is often called surface mount technology [46]. As electronic devices and its structure becomes more complex, so also the increasing component densities, increases [47]. In order to keep electronic performance and packaging size reasonably attractive, it is important to keep the lead pitch size at 0.65 mm or lesser.

Hermetic packaging materials have equally been used in other engineering applications in area where heat must be dissipated from the electronic device [48]. This can be noticed in small integrated electronic circuits with low lead count and also in electromagnetic shielding. In order for electronic devices to adopt hermetic packaging material, such device mush have a minimal leak rate i.e., the intensity at which heat can penetrate into or out of the packaging material. As global population rises, so also the producers and users of electronic devices increase the production capacity worldwide [49].

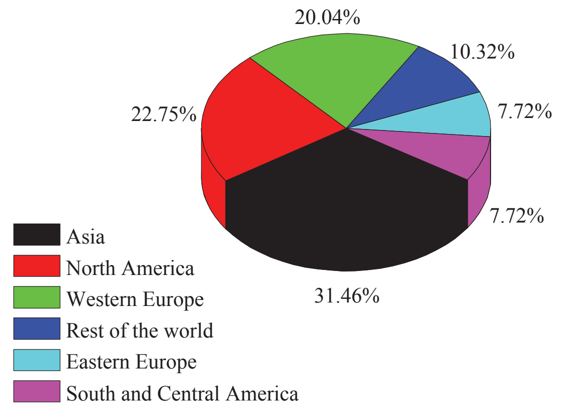

Figure 1: Global Application of Non-hermetic Packaging materials.

3 Current Development in Electronic Packaging Materials

The global demand of non-hermetic packaging materials is shown in Figure 1. It can be seen that the application of plastic or non-hermetic materials transcend all facet of the world with the projection of attaining a high proportion in the next two decades.

Currently Asia has the highest consumption rate of non-hermetic materials followed by North America. Sun and his co-workers [50] have also shown that hermetic materials may equally find useful application in other engineering application going by the trend depicted in Figure 2. Non-hermetic packaging materials continue to dominate packaging industries in view of its peculiar properties. Part of its attractive properties is the low thermal conductivities value compared with the hermetic materials. This property allows the retention of heat transfer within the conductor thereby limiting the heat dissipation through the insulator.

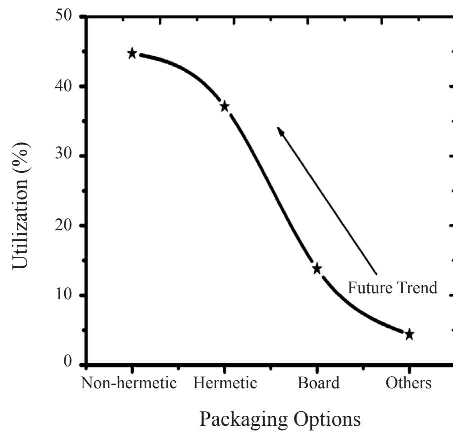

Figure 2: Future trends in Packaging Industry.

The application of hermetic materials is currently being noticed in military formation because of their perceived advantage over plastic in that specific area. One of the dominant property of hermetic materials over non-hermetic packaging materials is that most hermetic packages can be made nearly impervious to moisture when hermetically sealed. This may not be the case for non-hermetic materials most especially when the reinforcing fibre is made of natural fibre. This new approach is meant to reinforce electronic design and conductor chips, circuits and systems. The evolving roadmap for sustainable packaging, which came to limelight through system integration is meant to reduce the weight of all stages of electronic packaging. This was also corroborated by Szendiuch affirming that the electronic industry is currently reducing dimensions of packaged components as well as entire electronics systems [51]. To achieve this purpose, Surface Mount Device (SMD) passives and semiconductor chips are mounted in closed unit bringing together a functional system with improved reliability and affordable price.

This idea is intended to achieve reliable and cost effective system, where the size and weight of the packaging materials is reduced with lower voltages and higher speeds [52]. For instance, the typical size of surface mount device passives in 30 years ago was 1206 when they were first introduced in the market. Current developments in the industry has shown that all electronic components including electrical devices are now becoming miniaturized and smaller [53]. The industry is now moving toward a smaller size of 0201 and 01005 for passives while newly introduced fine pitch packages are being used for actives. Another improvement in electronics packaging is System On Package (SOP) where all components are placed in three-dimensional configuration [54]. Modern approach in electronics packaging requires miniaturized products especially in three dimensional configuration.

Moreover, it is required that quality and cost must be balanced. Consequently, this approach involves all components and semiconductor chips to be placed inside the system as it is in three-dimensional configuration. Although, this process may involve all kinds of problems – electrical (signal processing), physical (heat transfer and cooling), mechanical, chemical and also technological. The technological design is expected to evolve small connections and interconnection in order to process high density circuits while retaining a competitive cost.

4 Future Packaging Trends

Electronic packaging is currently taking various dimension with the development of two-dimensional packaging concept and the newly introduced three-dimensional (3-D) packaging [55]. Proponents of three-dimensional packaging have reported that apart from the increased electrical performance provided by this technology, packaging density tends to be increased compared to two-dimensional (2-D) approaches which have been used for a long period of time [56]. Conclusions drawn from related published works show that three dimensional packaging with its interconnection can increase system density by a factor of more than fifty by stacking integrated circuits [57], [58]. This may not be in the interest of weight saving potential when compared with two-dimensional packaging approach. Proponents of 2-D have based their arguments on the increased weight imposed using 3-D packaging. Figure 3 shows the integrated time path and improved generations of electronic packaging stages as reported in literature. This concept x-rays the migration from 2D component integration into heterogeneous system integration. Part of the distinguishing property of 3D-integration technologies can be found in homogeneous and in heterogeneous techniques.

The process of integration of dies into system devices with the same functionality is named homogeneous 3D-integration and is majorly used for memory stacks. This may not be said in heteroneous 3D-integration which combines dies of different

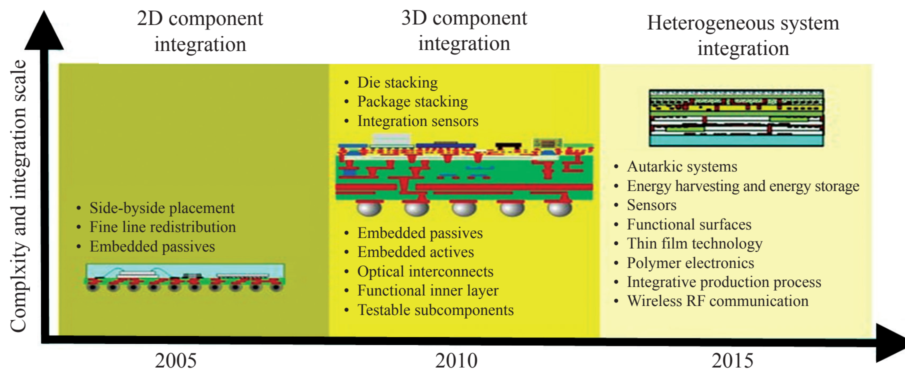

Figure 3: Future trends in Package technology [51].

applications like processors, sensors, memories and RF-components in one stack packages. The difficulties which have to be surmounted with respect to these wide range applications are as follows:

- die yield and its impact on 3D-integration,
- increment in component densities,
- availability of 3D design tools.

5 Conclusions

In this work, we have reviewed the broad concept of electronic packaging with much emphasis on the interface materials which is in this case represents the bridge between the insulation and the electronic devices. This work has also revealed the potentials of high temperature materials to dissipate excessive heat during high temperate weather condition. Key of the findings reported in this work showed that most polymeric materials with desirable high temperature properties has the potential to provide sustainable packaging for electronic devices. It is also shown that electronic packaging is changing from existing high temperature materials to 2-D system packaging, 3-D packaging. The overall objective of this concept is to evolve package integration leading to multi-functional systems in the interim with the aim of achieving mega-function systems in the future.

Findings from other works has shown that the increasing cost of 3D packaging materials may retard the spate of progress in this application. The cost will continue to be a major driving force in the advancement of technology globally, and will also have its share in electronic packaging industry. If the new integrated technology cannot achieve cost reduction compare with the existing packaging materials, then its acceptance will be prolonged.

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